Lab 9

The objective of this lab is to design multicore processor ( cache ) and test it using ModelSim altera quartus software. The testing includes read hit, read miss, write hit, write miss. The miss cases are followed by the hit since there are no blocks initialized in the cache initially. When there is a miss, the blocks of data will be initialized in the cache and after that, there will be read hit or write hit. Read hit and read miss are completed in this lab. Write hit and write miss have successful stalls but have a few bugs implementations.